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Question Paper Code : 80499

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Fourth Semester

Electrical and Electronics Engineering

EE 2255/EE 46/10133 EE 406 A/080280029 – DIGITAL LOGIC CIRCUITS

(Regulations 2008/2010)

(Common to PTEE 2255–Digital Logic Circuits for B.E. (Part-Time) Third Semester
Electrical and Electronics Engineering – Regulations 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by non weighted codes?
2. List the names of universal gates.
3. What is the drawback in RS flipflop?
4. Write the excitation table for D flipflop.
5. What is state assignment problem?
6. What are the benefits of state reduction?
7. What is the difference between PROM and EPROM?
8. What are the advantages of CMOS?
9. What are the advantages of VHDL?
10. What are the objectives for choosing test benches?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Prove that $F = \overline{A}.B + A.\overline{B}$ is exclusive OR operation and it equals $= \overline{(\overline{A.B})A.(\overline{A.B})B}$. (8)
- (ii) Prove that for constructing XOR from NANDs we need four NAND gates. (8)

Or

- (b) Simplify the Boolean function using Kmap $F(w, x, y, z) = \sum(1, 3, 7, 11, 15)$, which has the don't care conditions $d(w, x, y, z) = \sum(0, 2, 5)$. (16)
12. (a) A sequential circuit has two JK flip flops A and B. The flip flop input functions are:

$$J_A = B \quad J_B = \bar{x}$$
$$K_A = B\bar{x} \quad K_B = A \oplus x$$

- (i) Draw the logic diagram of the circuit (5)
- (ii) Tabulate the state table (6)
- (iii) Draw the state diagram. (5)

Or

- (b) Using JK flip flops, design a synchronous counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000. (16)
13. (a) Design mod 5 asynchronous counter. (16)

Or

- (b) Design a binary UP-DOWN ripple counter. (16)
14. (a) (i) Derive the PLA program table for a combinatorial circuit that squares a 3 bit number. Minimize the number of product terms. (8)
- (ii) An IC logic family has NAND gates with fanout of 5 and buffer gates with fanout of 10. Show how the output signal of a single NAND gate can be applied to 50 other gate inputs. (8)

Or

- (b) (i) Write notes on the characteristics of TTL and ECL logic families. (8)
- (ii) Design a ROM to convert 6 bit binary number to its corresponding 2-digit BCD number. (8)

15. (a) (i) Explain the function of the circuit specified by the following HDL code.

```
Module prob (A, B, S, E Q);
```

```
input [1: 0] A, B;
```

```
input S, E;
```

```
output [1 : 0] Q
```

```
assign Q = E? (S ? A : B) : 'bZ
```

```
end module.
```

(8)

- (ii) Write an HDL data flow description of a 4-bit adder subtractor of unsigned numbers. (8)

Or

- (b) Write the HDL code for ripple counter. (16)
